CLAIMS

We claim:

1. A method comprising:
commencing execution of a first set of one or more write instructions,
wherein the write instructions of the first set are the width of a processor data bus;
aborting the execution of the first set of write instructions;
creating a second set of one or more write instructions, in response to the aborting, wherein the write instructions of the second set are the width of an expansion bus; and
executing the second set of write instructions.

2. The method of claim 1, wherein the width of the processor bus is 32 bits.

3. The method of claim 1, wherein the width of the expansion bus is 16 bits.

4. The method of claim 1, wherein the second set of write instructions are suitable for transmission over the expansion bus.

5. A method comprising:
executing a write instruction that writes to a virtual memory address;
translating the virtual memory address, wherein translating includes
determining whether the virtual memory address maps to an inaccessible physical memory address;
generating an abort indication after determining that the virtual memory address maps to an inaccessible physical memory address;
performing the following in response to the abort indication,
creating multiple write instructions suited for transmission over an expansion bus; and

executing the multiple write instructions.

6. The method of claim 5, wherein the expansion bus is 16 bits wide.

7. The method of claim 6, wherein the write instruction is a 32-bit write instruction.

8. The method of claim 6, wherein the write instruction is wider than the expansion bus.

9. An apparatus comprising:

a memory management unit to receive a virtual address, the memory management unit to determine whether the virtual address maps to an inaccessible physical address and to transmit an abort indication if the virtual address maps to an inaccessible address; and

a processor core to receive the abort indication from the memory management unit and to execute instructions, the processor core including an abort handler to create new instructions in response to receipt of the abort indication, wherein the new instructions are the width of an expansion bus.

10. The apparatus of claim 9, wherein a physical address is inaccessible if it is write-protected.

11. The apparatus of claim 9 further comprising:

an external expansion device communicatively coupled to the processor core, the external expansion device to receive the new instructions over the expansion bus.

12. The apparatus of claim 11, wherein the expansion bus is 16 bits wide.

13. The apparatus of claim 9, wherein instructions are 32-bit instructions.

14. A system comprising:

a processor, the processor including,

a processor core to receive an abort indication, wherein the processor core includes an abort handler to create new write instructions suited for transmission over an expansion bus; and

a memory management unit (MMU) coupled to the processor core by a processor data bus, the MMU to determine whether a virtual memory address maps to an accessible physical memory address, the MMU to transmit the abort indication to the processor core if the virtual memory address does not map to an accessible physical memory address;

an external expansion device to receive the new write instructions from the processor over the expansion bus; and

a dynamic random access memory (DRAM) unit coupled to the processor, wherein the DRAM unit is to store data accessible by the processor.

15. The system of claim 14, wherein the expansion bus is half the width of the processor data bus.

16. The system of claim 14, wherein the abort indication includes the virtual memory address.

17. The system of claim 14, wherein the external expansion device is a flash memory device.

18. A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

commencing execution of a first set of one or more write instructions, wherein the write instructions of the first set are the width of a processor data bus;

aborting the execution of the first set of write instructions;

in response to the aborting, creating a second set of one or more write instructions, wherein the write instructions of the second set are the width of an expansion bus;

executing the second set of write instructions.

19. The machine-readable medium of claim 18, wherein the width of the processor bus is 32 bits.

20. The machine-readable medium of claim 18, wherein the width of the expansion bus is 16 bits.

21. The machine-readable medium of claim 18, wherein the second set of write instructions are suitable for transmission over the expansion bus.

22. A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

executing a write instruction that writes to a virtual memory address;

translating the virtual memory address, wherein translating includes determining whether the virtual memory address maps to an inaccessible physical memory address;

after determining whether the virtual memory address maps to an inaccessible physical memory address, generating an abort indication;

receiving the abort indication, and

creating multiple write instructions suited for transmission over an expansion bus; and

executing the multiple write instructions.

23. The machine-readable medium of claim 22, wherein the expansion bus is 16 bits wide.

24. The machine-readable medium of claim 22, wherein the write instruction is a 32-bit instruction.

25. The machine-readable medium of claim 22, wherein the write instruction is wider than the expansion bus.